

HFA1149 SPICE Macromodel (CFA)

Application Note

March 1997

MM1149

Introduction

The HFA1149 is a high speed, low power current feedback amplifier with output Enable/Disable capability. The macromodel for the HFA1149 is PSPICE (registered trademark of MicroSim Corp.) compatible, and may be compatible with other simulation programs as well. The model file is in ASCII format and may be viewed/edited with any text editor. For this model to run properly in PSPICE be sure to set ITL4 = 100 and turn on STEPGMIN; otherwise, convergence errors may occur.

All models require a trade-off between accuracy and complexity (simulation time). Intersil's models emulate the nominal performance of a typical device, and are designed to match the typical performance curves in the device data sheet.

SPICE simulations should not be considered a substitute for breadboarding a circuit; rather, they should be used to select preliminary component values and to verify the validity of a design approach.

Do not rely on simulations to predict device performance when deviating from the operating conditions specified in the data sheet (e.g., just because the model works with $\pm 1V$ supplies, don't assume that the actual amplifier does). Instead, refer to the data sheet performance curves, or call the factory for assistance (321-724-7143).

The HFA1149 model is configured as a subcircuit for easy incorporation into larger circuit files. When using PSPICE, call a subcircuit from the top level circuit file by adding a .LIB statement to point to the file containing the subcircuit (e.g. .lib c:\models\hfa1149.cir), and by including a subcircuit call of the following form:

model xname +IN -IN V+ V- DIS THR POLOUT name (e.g., x22 106 107 109 110 111 112 113 108 op amp)

Note that the node order in the subcircuit call follows the industry standard, and the order is also documented in the comment section at the beginning of the model file.

Model Description

The macromodel schematic is shown in Figure 1, and the PSPICE listing for the macromodel follows. The HFA1149 model is basically the HFA1109 amplifier model with circuitry around it to implement the output Enable/Disable function.

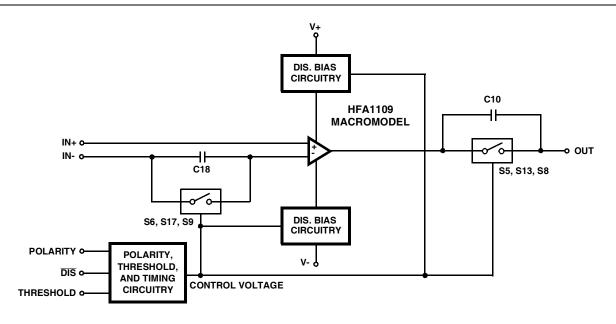
The model topology consists of three main functional sections: a buffer between the two input pins, an output section between the inverting input pin and the output pin, and an enable section.

The input buffer section is a unity gain buffer with additional components added to model the critical characteristics of the actual buffer. Of these additional components, some are used to model both the slew limiting of the inverting input and the fractional step feed-through from the noninverting input to the inverting input. Other elements model the voltage and current limiting of the inverting input. The bias current of the non-inverting input and the high frequency voltage gain are also accounted for in the input buffer section.

The output section is a transimpedance amplifier constructed from four stages: current probe, mid stage, frequency transfer, and output drive. The current probe stage monitors the current through the inverting input pin and also models the input offset voltage. The mid stage is used for the bias current of the inverting input and for power supply gains. The frequency transfer block consists of two poles and two zeros for modeling the high frequency openloop transimpedance gain. The output drive stage accounts for several characteristics including: the output slew limits and resulting transimpedance gain bandwidth product, the saturation delay times, and the voltage and current limiting at the output.

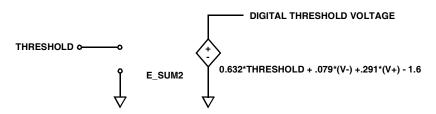
The enable section accurately models the turn-on/turn-off times, disabled I_{cc} , and off-isolation. This section operates according to the voltage level at the disable input pin which controls the input/output impedance and the Enable/Disable time of the amplifier. The internal bias current of the input buffer section is also set by the enable section shown at the bottom of Figure 1C. As a result, high impedance states are achieved at the two input pins whenever the amplifier is disabled. The polarity function was implemented with the circuitry at the bottom of Figure 1B and the threshold pin functionalities were modeled with the circuitry at the top of Figure 1B.

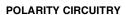
In addition to the three main functional sections, smaller constructs and individual components are used to model other important amplifier characteristics. Specifically, one section is used to capture the change in the voltage limits of the output as a function of the current through the inverting input.

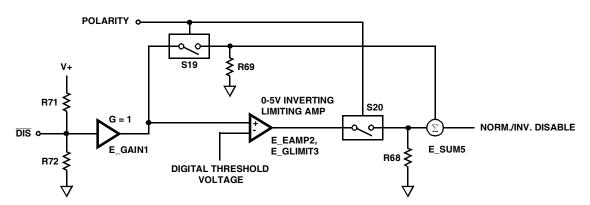




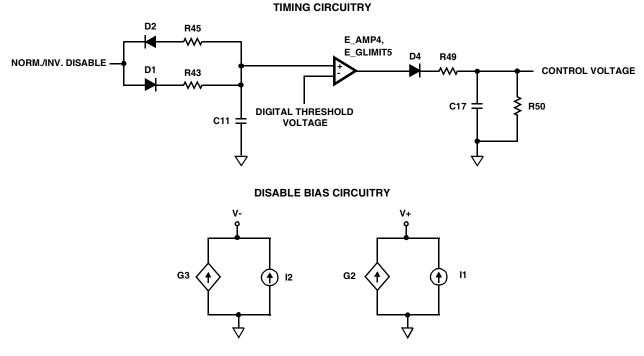
THRESHOLD CIRCUITRY



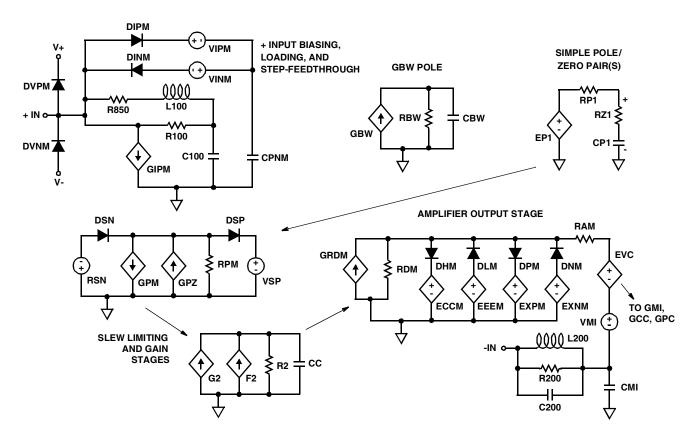




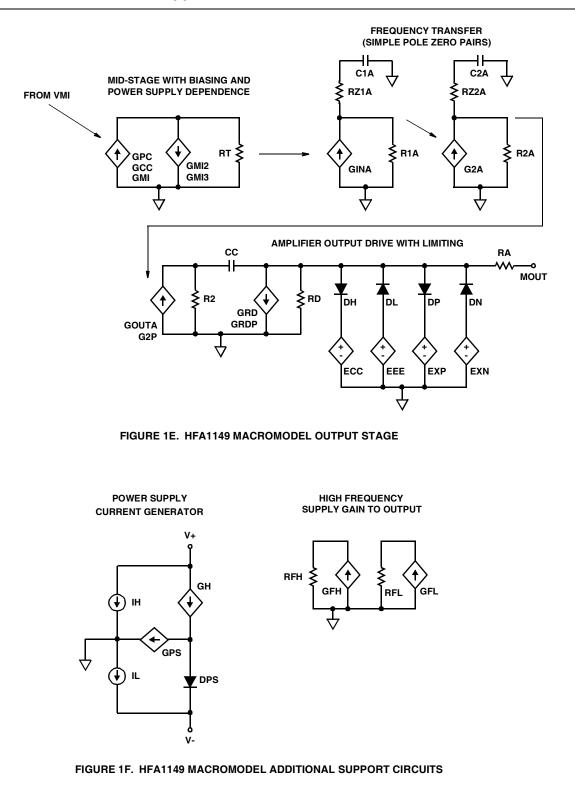












HFA1149 SPICE Macro Model Listing

* Copyright (C) 1997 Intersil Corp. * Rev. 2/24/97, Be sure to set ITL4=100 and turn on STEPGMIN for PSpice to simulate properly. *Subcircuit Call Order: +IN -IN V+ V- DISABLE THRESHOLD POLARITY OUT .SUBCKT HFA1149 + - V+ V- DIS_ THR POL OUT 1 2 V+ V- 3 HFA1109AMP X_U10 S S5 5 OUT in2 4 Switch2 RS_S5 in2 4 1G S_S6 7 - in2 6 Switch2 RS_S6 in2 6 1G V_V38 40.5 V V39 60.05 S_S8 9 2 8 in 2 Switch 2 RS_S8 8 in2 1G V V42 802.0 S_S9 11 0 10 in2 Switch2 RS_S9 10 in2 1G V V43 1002.0 D D1 12 13 Dlow V_V45 140.5 D D2 15 12 Dlow D_D3 14 16 Dlow E EAMP1 17 0 VALUE = { V(18, 19)*1 } D D4 20 21 Dlow S_S13 3 5 in2 22 Sout4 **RS_S13** in2 22 1G V_V52 220.1 V_V54 230.5 S S17 7 2 in2 23 Sout4 RS_S17 in2 23 1G V_V59 240.5 I_I1 0 V+ DC 6.6mA 1 12 0 V- DC -6.6mA R_R40 93 250 R_R42 11 25 90 R_R43 13 18 13k C_C11 14 18 5p R_R44 14 18 100k C_C12 18 15 1p IC=0 R_R45 15 18 10 R_R46 16 18 1 R_R49 in2 21 10 R_R50 in2 0 1.5k C_C17 0 in2 5p R_R51 24 18 10e6 C_C10 OUT 5 .025p C_C18 2 - .025p G_G2 0 V+ 12 0 -1.32e-3 G_G3 0 V-12 0 1.32e-3 E_SUM2 19 0 VALUE {.291*V(26)+.079*V(27)+.632*V(THR)+V(28)} V_V73 280-1.6 S_S18 2 25 29 0 Switch6 **RS_S18** 29 0 1G S_S19 30 31 POL 0 Sdisable **RS_S19** POL 0 1G 33 34 32 POL Sdisable S_S20 **RS_S20** 32 POL 1G E_SUM5 12 0 VALUE {V(30)+V(33)} R_R68 0331k R R69 0301k

V CONST2 32 0 DC 3.000 35 0 VALUE {1 * V(DIS_)} E_GAIN1 R_R71 DIS_V+ 50k R_R72 0 DIS_ 5e6 R R73 POL V+ 50k R R75 THR 36 50k V_V84 3603 **R_R76** 0 THR 5e6 **R_R77** 0 POL 5e6 R R80 26 V+ 1 R R81 V-27 1 R_R82 0 26 5e6 R_R83 27 0 5e6 E_EAMP2 37 0 VALUE = { V(35, 19)*-1 } E_GLIMIT3 34 0 VALUE {LIMIT(V(37)*50,0,5)} R R84 034 1k E_GLIMIT2 20 0 VALUE {LIMIT(V(17)*50,0,5)} E ABS4 29 0 VALUE {ABS(V(1))} R_R86 +11 R_R87 10 10e6 E_EAMP4 38 0 VALUE = { V(35, 19)*1 } E GLIMIT5 31 0 VALUE {LIMIT(V(38)*50,0,5)} .model Dlow D N=.01 .model Switch6 VSWITCH Roff=300 Ron=1 von=1.0 voff=1.1 .model Sdisable VSWITCH von=2 voff=1 .model Sout4 VSWITCH Ron=.1 Roff=10k von=3.5 voff=.1 .model Switch2 VSWITCH Roff=10e6 Ron=.1 von=.2 voff=.1 .ENDS HFA1149 .SUBCKT HFA1109AMP 106 107 109 110 108 L200 111 107 +1.6000000E-05 R200 111 107 +1.18000000E+02 C200 107 111 +1.3000000E-12 L100 101 850 +5.0000000E-07 R100 101 106 +4.50000000E+03 C100 101 0 +3.100000000E-13 R850 106 850 75 VMI 111 112 +0.0000000E+00 GINIH 0 113 109 0 1M R1IH 113 0 1K C1IH 113 0 +1.59159637E-13 R2IH 114 0 -1.00000000E+03 RY2IH 114 115 +1.0000000E+03 C2IH 115 0 +4.82301931E-11 G2IH 0 114 113 0 -1.0000000E-03 GOUTIH 116 0 114 0 -1.0000000E+00 RPGIH 116 0 1 GINIL 0 117 110 0 1M R1IL 117 0 1K C1IL 117 0 +1.59159637E-13 R2IL 118 0 -1.0000000E+03 RY2IL 118 119 +1.0000000E+03 C2IL 119 0 +8.37682301E-11 G2IL 0 118 117 0 -1.0000000E-03 GOUTIL 120 0 118 0 -1.00000000E+00 **RPGIL 120 0 1** EVC 121 112 POLY 4 106 0 111 0 116 0 120 0 -2.76409908E-03 ++2.23336645E-04 +2.23336645E-04 +8.08400638E-05 -5.27513353E-04 0 0 +-7.70216445E-06 +7.70216445E-06 0 -7.70216445E-06 +7.70216445E-06

++7.70216445E-06 0 -7.70216445E-06 CMI 111 0 +1.0000000E-15 FPM 122 0 VMI +1.00000000E+00 DMP 122 123 DIM DMM 124 122 DIM .MODEL DIM D IS=1E-16 N=.001 GCC 122 0 POLY 4 106 0 111 0 109 0 110 0 +6.58458515E-06 +4.90772982E-07 ++4.90772982E-07 -1.08867981E-07 +1.09041394E-06 0 0 +1.74372872E-08 +-1.74372872E-08 0 +1.74372872E-08 -1.74372872E-08 -1.74372872E-08 0 ++1.74372872E-08 VMP 123 0 0 VMM 0 124 0 FMI 0 103 POLY 2 VMP VMM 0 -9.0000000E-03 +9.0000000E-03 RT 103 0 +1.0000000E+00 GPC 0 103 POLY 2 109 0 110 0 0 +0.00000000E+00 +0.00000000E+00 GINA 0 125 103 0 1M R1A 125 0 1K C1A 125 0 +1.59159637E-13 G2A 0 126 125 0 1M R2A 126 0 1K C2A 126 0 +5.89480137E-14 G3A 0 127 126 0 1M R3A 127 0 1K C3A 127 0 +3.97899093E-15 R4A 128 0 +1.0000000E+03 RY4A 128 129 -1.0000000E+03 C4A 129 0 +2.65266062E-14 G4A 0 128 127 0 +1.0000000E-03 R5A 130 0 +1.0000000E+03 RY5A 130 131 -1.0000000E+03 C5A 131 0 +2.27370910E-14 G5A 0 130 128 0 +1.0000000E-03 GI6A 0 132 130 0 +2.0000000E-03 R6A 132 0 +1.0000000E+03 C6A 132 0 +5.82692545E-14 G6A 0 132 133 0 -1.0000000E-03 GY6A 0 133 132 0 1M CY6A 133 0 +3.39618104E-13 RY6A 133 0 1K RO6A 0 134 1e9 R7A 134 135 +5.02412563E+05 GI7A 0 134 133 0 +1.99000000E-06 C7A 134 135 +4.28082941E-14 G7A 0 135 136 0 -1.0000000E-03 GY7A 0 136 135 0 1M CY7A 136 0 +1.08077511E-14 RY7A 136 0 +1.0000000E+04 GZ7A 0 137 134 0 -1.0000000E-06 RZ7A 137 0 -1.0000000E+06 RC7A 137 138 1000001 CZ7A 138 0 +2.15074248E-14 GOUTA 105 0 137 0 -1.00000000E+00 GRD 102 0 105 0 +4.27868630E+00 GINOH 0 139 109 0 1M R10H 139 0 1K C1OH 139 0 +1.59159637E-13 GOUTOH 140 0 139 0 -1.00000000E+00 RDPH 140 0 1 GINOL 0 141 110 0 1M

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R10L 141 0 1K C1OL 141 0 +1.59159637E-13 GOUTOL 142 0 141 0 -1.0000000E+00 RDPL 142 0 1 G2P 0 105 POLY 2 140 0 142 0 0 +1.38629436E-07 +1.38629436E-07 GRDP 102 0 POLY 2 140 0 142 0 0 -2.20878759E+00 -2.20878759E+00 R2 105 0 +3.60673760E+06 CC 105 102 +1.0000000E-14 RD 102 0 +7.2000000E+00 RA 102 108 +1.07000000E+01 DH 102 104 DH +1.0000000E+00 DL 100 102 DL +1.0000000E+00 .MODEL DH D IS=+1.99173432E-14 N=.2 .MODEL DL D IS=+1.28277200E-14 N=.2 ECC 104 0 POLY 2 109 0 143 0 -1.19000000E+00 1 1 EEE 100 0 POLY 2 110 0 144 0 +1.25000000E+00 1 1 FCC 0 143 POLY 1 VMI +9.96717960E-05 +1.33000000E-01 RCC 143 0 1K CRC 143 0 +1.0000000E-10 D55 143 0 DLIMVO FEE 0 144 POLY 1 VMI -1.63095844E-04 +1.63000000E-01 REE 144 0 1K CRE 144 0 +1.0000000E-10 D66 0 144 DLIMVO .MODEL DLIMVO D N=.01 IS=1E-20 DP 102 145 DCL +1.0000000E+00 EXP 145 0 POLY 2 102 0 108 0 0 +3.20491434E-01 +6.77833280E-01 DN 146 102 DCL +1.0000000E+00 EXN 146 0 POLY 2 102 0 108 0 0 +1.86957037E-01 +8.11038456E-01 .MODEL DCL D IS=1E-9 N=1 IPS 109 110 +9.4000000E-03 GPS 147 0 102 108 +9.34579439E-02 GH 109 147 POLY 1 147 110 +1.61343210E-02 -3.22686420E-02 +2.42014815E-02 +-8.06716049E-03 +1.00839506E-03 DPS 147 110 DPS .MODEL DPS D IS=1E-16 N=+3.40072108E+00 DVPM 106 109 DLIMM GIPM 106 0 POLY 4 106 0 111 0 109 0 110 0 -5.30320265E-06 +1.02950000E-05 +-9.70500000E-06 -2.95000000E-07 -2.95000000E-07 **DVNM 110 106 DLIMM** VIPM 148 149 0 DIPM 106 148 DLIMM **DINM 150 106 DLIMM** VINM 149 150 0 CPNM 149 0 +1.0000000E-15 RINM 106 101 +1.0000000E+04 CINM 101 0 +9.9000000E-14 GINI 0 151 106 0 1M R1I 151 0 1K C1I 151 0 +1.90382341E-13 GI2I 0 152 151 0 +1.12250000E-03 R2I 152 0 +8.16326531E+03 C2I 152 0 +9.96948751E-14 G2I 0 152 153 0 -1.0000000E-03 GY2I 0 153 152 0 1M CY2I 153 0 +1.61679590E-12 RY2I 153 0 1K G3I 0 154 153 0 1M R3I 154 0 1K

C3I 154 0 +7.76388474E-13 G4I 0 155 154 0 1M R4I 155 0 1K C4I 155 0 +5.30532124E-14 G5I 0 156 155 0 1M R5I 156 0 1K C5I 156 0 +5.30532124E-14 R6I 157 0 -1.0000000E+03 RY6I 157 158 +1.0000000E+03 C6I 158 0 +1.76844041E-13 G6I 0 157 156 0 -1.0000000E-03 R7I 159 0 -1.0000000E+03 RY7I 159 160 +1.0000000E+03 C7I 160 0 +8.37682301E-14 G7I 0 159 157 0 -1.0000000E-03 R8I 161 0 -1.0000000E+03 RY8I 161 162 +1.0000000E+03 C8I 162 0 +8.37682301E-14 G8I 0 161 159 0 -1.0000000E-03 R9I 163 0 -2.0000000E+03 RZ9I 163 164 +3.0000000E+03 C9I 164 0 +5.30532124E-14 G9I 0 163 161 0 -5.0000000E-04 R10I 165 0 -2.0000000E+03 RZ10I 165 166 +3.0000000E+03 C10I 166 0 +5.30532124E-14 G10I 0 165 163 0 -5.0000000E-04 R11I 167 0 -2.0000000E+03 RZ11I 167 168 +3.0000000E+03 C11I 168 0 +5.30532124E-14 G11I 0 167 165 0 -5.0000000E-04 R12I 169 0 -2.0000000E+03 RZ12I 169 170 +3.0000000E+03 C12I 170 0 +5.30532124E-14 G12I 0 169 167 0 -5.0000000E-04 R13I 171 0 -2.0000000E+03 RZ13I 171 172 +3.0000000E+03 C13I 172 0 +5.30532124E-14 G13I 0 171 169 0 -5.0000000E-04 R14I 173 0 -2.0000000E+03 RZ14I 173 174 +3.0000000E+03 C14I 174 0 +5.30532124E-14 G14I 0 173 171 0 -5.0000000E-04 R15I 175 0 -2.0000000E+03 RZ15I 175 176 +3.0000000E+03 C15I 176 0 +5.30532124E-14 G15I 0 175 173 0 -5.0000000E-04 R16I 177 0 -2.0000000E+03 RZ16I 177 178 +3.0000000E+03 C16I 178 0 +5.30532124E-14 G16I 0 177 175 0 -5.0000000E-04 R17I 179 0 -2.0000000E+03 RZ17I 179 180 +3.0000000E+03 C17I 180 0 +5.30532124E-14 G17I 0 179 177 0 -5.0000000E-04 R18I 181 0 -2.0000000E+03 RZ18I 181 182 +3.0000000E+03 C18I 182 0 +5.30532124E-14 G18I 0 181 179 0 -5.0000000E-04

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HFA1149 SPICE Macro Model Listing (Continued)
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GOUTI 183 0 181 0 -1.00000000E+00 GPMM 183 0 184 0 +1.00200401E+00 RPMM 183 0 +1.12142857E+11 VSPM 185 0 +9.64285714E-01 **DSPM 183 185 DLIMM** VSNM 0 186 +1.03571429E+00 **DSNM 186 183 DLIMM** .MODEL DLIMM D N=0.01 G2M 187 0 POLY 2 183 0 184 0 0 +1.0000000E-03 +1.0000000E-03 F2M 187 0 POLY 2 VIPM VINM 0 +1.25000000E+02 -1.25000000E+02 R2M 187 0 1 CCM 187 184 +1.78571429E-12 G4M 184 0 187 0 1K R4M 184 0 1 GRDM 0 188 184 0 +1.14652603E-02 RDM 188 0 +8.72200000E+01 RAM 188 121 +1.78000000E+00 DHM 188 189 DVM +1.0000000E+00 DLM 190 188 DVM .MODEL DVM D IS=1E-16 N=.2 ECCM 189 0 POLY 1 109 0 -2.83000000E+00 1.0 EEEM 190 0 POLY 1 110 0 +2.83000000E+00 1.0 DPM 188 191 DCLM +1.0000000E+00 EXPM 191 0 POLY 4 188 0 121 0 109 0 110 0 0 -5.28714965E+01 +5.38520064E+01 + +9.74504713E-03 +9.74504713E-03 DNM 192 188 DCLM +1.0000000E+00 EXNM 192 0 POLY 2 188 0 121 0 0 -8.28974671E+01 +8.38903217E+01 .MODEL DCLM D IS=1E-20 N=1 FPS 0 147 VMI 1 .ENDS HFA1109AMP

HFA1149 Macro Model Performance

The model is designed for operation at \pm 5V. Beware, the model does not simulate various breakdown conditions such as exceeding the maximum ratings, but it does have input limiting. The model does not include input voltage or current noise, or temperature effects. The poles and zeros of the transimpedance frequency transfer section have been located with great care to insure that the performance for three different gains is matched closely to the curves given in the data sheet. Also, the pole/zero placement insures that the transient response matches that shown in the data sheet.

Intersil Application Note AN9523 titled "Evaluation Programs For SPICE Op Amp Models" was used as a guideline for evaluating the HFA1149 performance. Figure 2 shows the AC transfer function for gains of 2, 1, and -1. In the gain of two configuration the peaking is 0dB versus the 0dB of peaking shown in the data sheet. The gain of two simulated -3dB bandwidth is 430MHz compared to the data sheets 450MHz. This is quite a good correlation between the model and the data sheet. Similarly, the gains of 1 and -1 have -3dB bandwidths of 325MHz and 390MHz which closely match the 330MHz and 375MHz listed in the data sheet. The large signal responses for gains of 1 and 2 are shown in Figure 3 and the response for a gain of 2

slew rate versus the data sheets $1100V/\mu$ s, and it shows a $600V/\mu$ s gain of 1 slew rate versus the data sheet's $575V/\mu$ s. Figure 4 shows a $2900V/\mu$ s slew rate for the gain of -1 versus the data sheet's $2600V/\mu$ s. Again the correlation between the model and the data sheet is quite good. The small signal pulse responses are shown in Figures 5 and 6. The rise time, fall time, and overshoot can be read off these waveforms. Figure 7 is a graph of the off-isolation which correlates closely to the data sheet's -54dB at 30MHz and -64dB at 10MHz. Figures 8 and 9 correspond to the large signal and small signal enable/disable time. The enable and disable times are accurately modeled but the enable overshoot does not match the data sheet specifications.

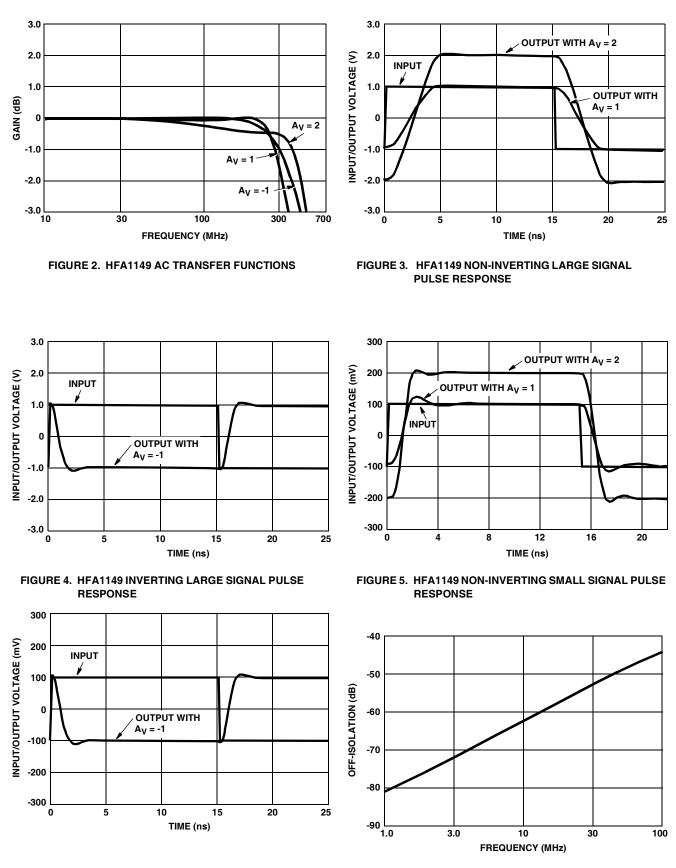


FIGURE 6. HFA1149 INVERTING SMALL SIGNAL PULSE RESPONSE



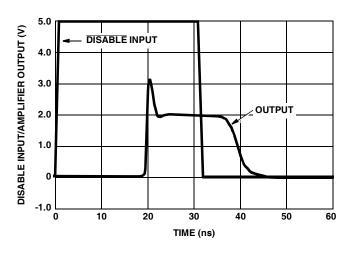


FIGURE 8. HFA1149 LARGE SIGNAL ENABLE/DISABLE TIME WITH AV = 2 AND VIN = 1V

Summary

The macromodel performs well for both the DC and AC parameters. It is a fraction of a dB off for some AC tests, but this is acceptable for an approximation. At least the model has peaking where the op amp has peaking, and the response for different gains is modeled correctly. The model is just an approximation! It cannot predict performance to a few percent; especially when one considers that the circuit layout parameters have such a large effect on high frequency performance. The model will not predict the actual performance in many circumstances such as non-linearities, limits of performance, or extended range operation. Only testing will confirm performance out of the normal operating range, and all circuits should be tested to confirm the model's predictions.

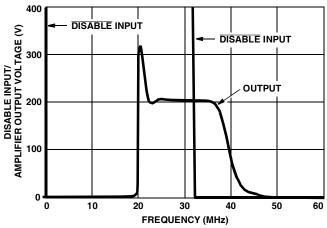


FIGURE 9. HFA1149 SMALL SIGNAL ENABLE/DISABLE TIME WITH $A_V = 2$ AND $V_{IN} = 0.1V$

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